Fringe modulation for an MROI beam combiner

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ABSTRACT

We report on the testing of the modulators within the MROI fringe tracking beam combiner. Modulation in the beam combiner will be performed via modulators introducing an optical path difference in increments of $\lambda/4$ into the beams. Knowledge of the path difference introduced needs to be accurate to within 1%. To achieve this accuracy, the modulators are characterized and the desired step waveform optimized through a Fourier analysis technique. Control is implemented in an FPGA embedded system and performance will be monitored by means of a slow loop Fourier algorithm. Details of the progress on characterization, optimization and future implementation are presented here.

Keywords: MROI, optical interferometry, fringe tracking, fringe modulator, fringe modulation

1. INTRODUCTION

To aide in correction for atmospheric aberrations at the MROI,[1] a temporal modulation of the input beams is used. The modulation is done with a bank modulators introducing a known optical path difference (OPD) into the optical train. This will take place in the dedicated fringe tracking beam combiner. It was shown by Thorsteinsson and Buscher that piezoelectric actuators or modulators are stable to fringe modulation waveforms over an extended period of time given a properly optimized waveform.[2] If a suitable frequency response of the system is found, optimization of the modulation waveform can be done in the frequency domain.

The optical layout of the beam combiner is shown in Figure 1 with the bank of modulators circled. Through modelling the fringes produced by the beam combiner, the group delay can be estimated and offset corrections applied to the delay lines. A simplistic overview of how the fringe tracker achieves this using inputs from three telescopes is shown in Figure 2. The three inputs are fed into the beam combiner from the switch yard producing two complementary sets of outputs. Each set of outputs are then separately dispersed by spectrographs into spectral channels onto detectors. Once the detectors have been read, the inputs are modulated by $\pi/2$ radians and the process starts over. Because the two outputs are π radians out of phase, each read of the detectors corresponds to an A and C or B and D measurement in the A, B, C, D modulation scheme.[3] After the initial read, fringes can modelled, the group delay estimated and corrections applied to the delay lines on subsequent reads.[4] For more information on the MROI fringe tracker and its subsystems, please refer to Jurgenson et al.[5]

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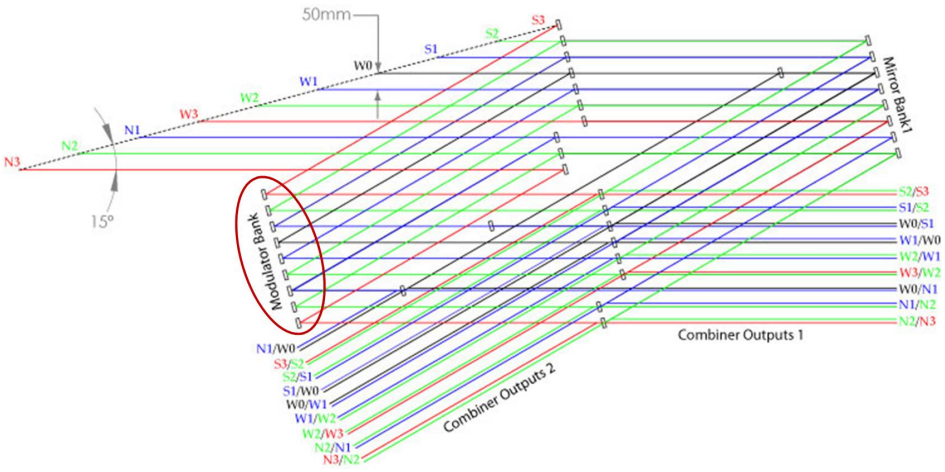

Figure 1. Optical layout of the fringe tracking beam combiner. The modulator bank is circled.

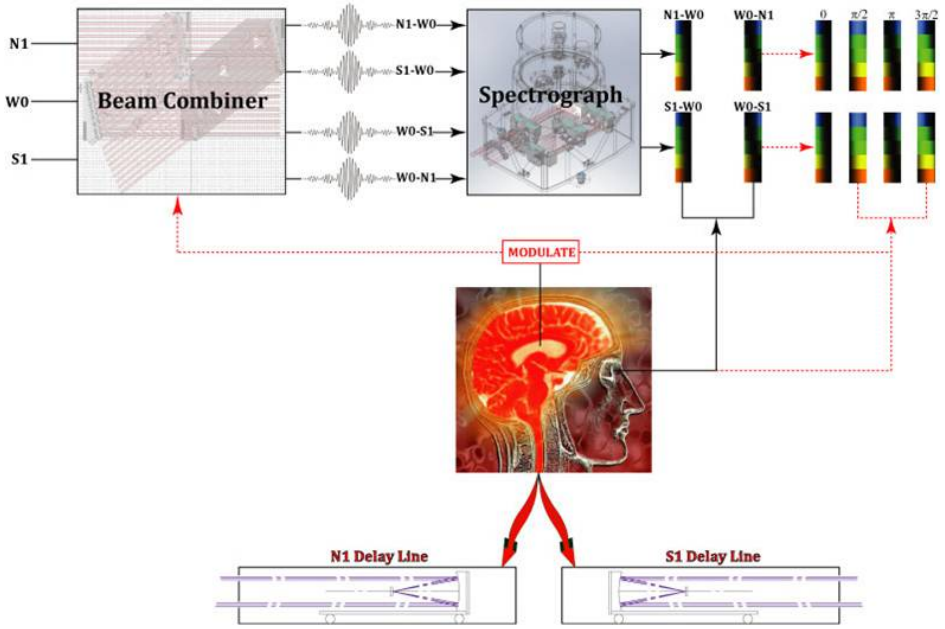

Figure 2. Overview of fringe tracking beam combiner operation using three telescopes. The three inputs produce two sets of complementary outputs that are dispersed by spectrographs onto detectors. Once the detectors have been read, offset corrections are applied to the delay lines, the inputs are modulated and the process starts over.

2. MODULATION STRATEGY

The desired $\pi/2$ phase shift in the outputs is accomplished by introducing an OPD of $\lambda/4$ into the beams. This is done by driving the modulators in a predefinded waveform. The ideal modulation waveform is shown in Figure 3 with the corresponding measurements taken by the detectors labeled for each step. At Position 0, A and C measurements are sampled. The detectors integrate for a time T_{int} while being sampled non-destructively a number of times determined by T_{int}/T_{sample}. After a time T_{hold}, the modulators are stepped a distance D_{mod} to Position 1 and B and D measurements are taken in the same manner. Measurements A and C are taken again at Position 2 but on different detectors. Once B and D have been acquired again at Postion 3, the modulators are stepped backwards and all measurements are taken again. This modulation strategy allows each detector to take all A, B, C and D measurements in both directions of modulator travel.[4]

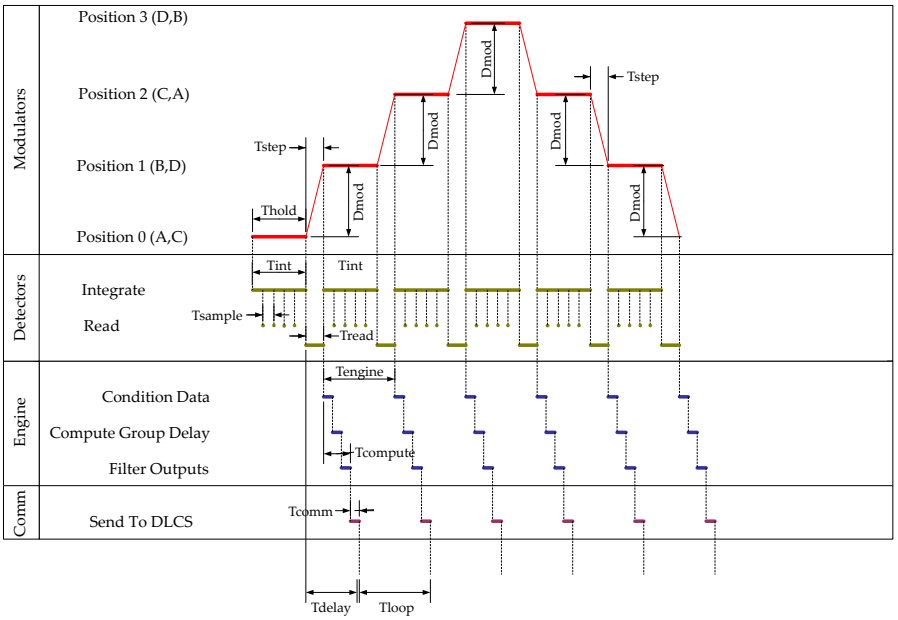

Figure 3. Modulation waveform and corresponding timing sequence. Measurements made by the detectors are labeled for each step. D_{mod} is dependent on the observing wavelength and T_{hold} will be a minimum of 5ms.

Due to the optical layout of the beam combiner shown in Figure 1, the 15^o incident angle from the switch yard results in the same for the modulators. Thus, to produce the desired OPD, the step size is given by

$$D_{mod} = \frac{\lambda}{8cos(15^o)}. \quad (1)$$

The fringe tracker will operate in the H or K_s band. Taking λ as 1.49μm, the shortest operating wavelength, D_{mod} becomes 192.8nm resulting in a total travel of 578.4nm for the waveform. To achieve the desired waveform accuracy of 1%, the modulator's position must be known to within 5.7nm. Corrections to the delay lines will be made after each step at a maximum rate of 200Hz making T_{hold} a minimum of 5ms.

3. EXPERIMENTAL SETUP

The current experimental setup is shown in Figure 4. A Xilinx ML510 FPGA board controls a Piezomechanik PC-AHV 150 DAC powering the modulator, a Piezomechanik STr-35 Mirror-shifter. The modulator has a strain gauge that is amplified and then sampled by an Advantech PCI-1714UL ADC.

3.1. Modulator

The modulator chosen was the Piezo Mirror-shifter STr-35/150/6 from Piezomechanik. It has an operating range of 0-150V with an advertised travel of 6μm. Preliminary tests found the total stroke to be closer to 9.5μm. There is a 35mm screw cap to which a 30mm mirror is expoxied to. To assure an even thickness between the mirror and screw cap, a jig was assembled for the gluing process and 130μm fishing line used as a spacer. No tests were done to determine parallelism. The modulator has an internal strain gauge that is amplified using a DMS 3 strain gauge amplifier from Piezomechanik. The DMS 3 outputs a 0-5V signal covering the entire stroke of the modulator and can be calibrated to adjust the zero position.

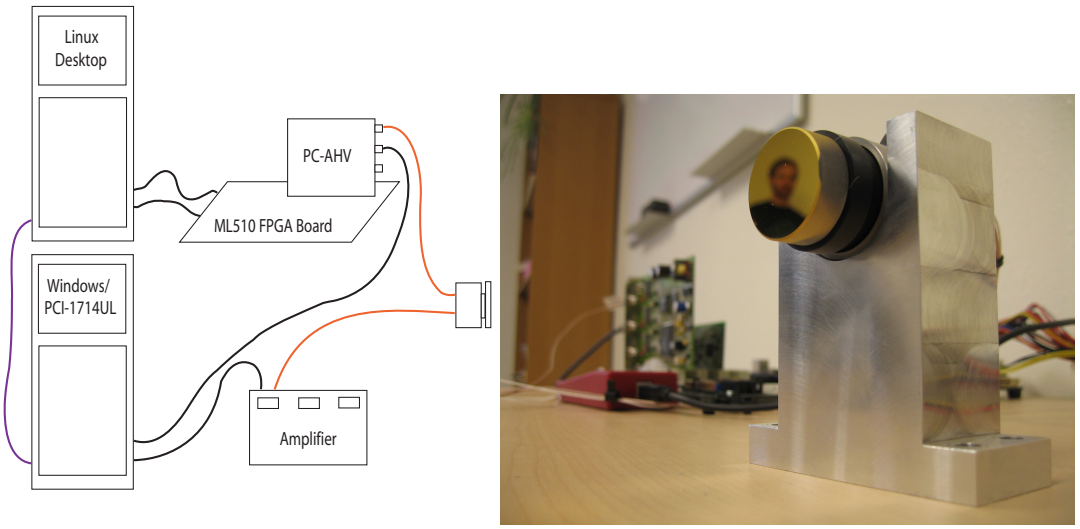

Figure 4. On the left is an overview of the present setup for the modulator characterization and optimization experiment. The right picture is the modulator and mirror in its mount for the experiment with the PC-AHV mounted on the FPGA board in the background.

3.2. Modulator Control

To power the modulator, a three channel Piezomechanik PC-AHV 150 DAC is used. The PC-AHV is a 5V PCI card with 14-bits of resolution and has an operating range of 0-150V. Initial tests showed the DAC possessed a slew-rate limiting characteristic. While holding the amplitude of the driving wave constant and increasing the frequency, the output wave would decrease in amplitude but still represented the driving wave. Assuming the modulator is linear over its 9.5μm range, the DAC will give a resolution of 0.58nm per LSB or 63.3nm per volt. Taking the advertised 50mV maximum noise level into account, the resolution becomes 3.15nm allowing for the desired 1% accuracy in modulator position to be achieved.

A Xilinx ML510 development board is used to control the DAC. The ML510 comes equipped with a Virtex 5 FXT FPGA that has two embedded PowerPC 440 processors in its fabric. Xilinx provides their own Linux distribution that was ported to one of the processors creating an embedded control system. Support for 5V PCI cards was originally disabled in the kernel. Enabling this required proper mapping of the interrupts from the PCI slots to the interrupt controller on the FPGA.[6] Once the kernel is downloaded and booted through a JTAG connection, further communication with the ML510 is done through an SSH server. The FPGA can be configured to boot from a CompactFlash card but this has not yet been attempted.

3.3. Waveform Generation and Sampling

Sampling of the strain gauge amplifier is done with an Advantech PCI-1714UL ADC. The PCI-1714 is a 12-bit, four channel card with an accuracy of ± 1 LSB. Assuming the 9.5μm stroke of the modulator transfers into the 5V range of the strain gauge amplifier, the ADC will have a resolution of $\pm$2.32nm putting it within the range of the 1% waveform accuracy criteria. Currently the ADC is mounted in a Windows desktop. Future implementation of the control system will address this issue.

Generation of the driving waveform is done by a program running under Linux on the FPGA. One period of the waveform is synthesized and written to a memory buffer where it is iterated over by a module on the FPGA, sending out the values over the PCI bus to the DAC. One channel of the DAC is used to trigger sampling on the ADC. Because each channel must be accessed separately over the PCI bus, there was a known adjustable latency between the trigger and start of the output built into the FPGA module that must be accounted for during analysis.

4. CHARACTERIZATION

It is advantageous to determine the frequency response of the system to identify any problematic driving frequencies that should be avoided. Ideally, the frequency response of the modulator and driving hardware would be isolated but because the motion of the modulator is only monitored through the strain gauge, its response will be present as well. The response curve is built point by point by writing a sine wave to the buffer, having the FPGA output it to the DAC and sampling the output from the strain gauge. A sine wave is a delta function in the frequency domain so the system response at the input frequency is found through the convolution theorem,

$$x(t) * \phi(t) = y(t) \tag{2}$$

$$\Phi(f) = \frac{Y(f)}{X(f)} \tag{3}$$

where $X(f)$ is the input, $\Phi(f)$ is the system response and $Y(f)$ is the output in the frequency domain. Lower case letters denote the time domain where the convolution turns into a pointwise multiplication in the frequency domain. The amplitude and phase information can then be determined from the complex response $\Phi(f)$. The input can be taken in two ways. Either the DAC directly sampled, or the waveform written to the buffer synthesized during analysis.

To avoid nonlinearities at the extremes of the modulator's operating range, an offset corresponding to 75V is added to the sine wave before writing it to the buffer. Because optimization will correct for both the modulator and driving hardware, the input, $x(t)$, is taken as the waveform written to the buffer. A rough frequency response curve has been obtained and is dominated by the slew-rate limiting characteristic of the DAC. As previously mentioned, there is a built in known delay between the trigger and subsequent output of the waveform to be accounted for.

5. OPTIMIZATION

With a frequency response found and any problematic frequencies identified, the ideal waveform can be optimized. Optimization will be done with an iterative algorithm outlined in Thorsteinsson and Buscher. By first breaking down the waveform in a Fourier series, a select number of components are chosen to synthesize the original wave. The ideal modulation waveform shown in Figure 3 can be expressed as

$$x(t) = \sum_{n=odd} \frac{2D_{mod}}{n\pi} \left[2sin\left(\frac{n\pi}{2}\right) cos\left(\frac{n\pi}{6}\right) cos\left(\frac{n\pi}{3T_{hold}}t\right) + sin\left(\frac{n\pi}{3T_{hold}}t\right) \right]. \tag{4}$$

To determine the number of components to use in the series, the resolution of the the DAC and ADC are considered. In the present setup, the limiting factor is the resolution of the ADC, 2.32nm. Taking D_{mod} as the previously mentioned 192.8nm for the shortest operating wavelength, the amplitude of oscillations on a step reach the resolution of the ADC at approximately 55 components (28 if counting only the odd components). The resulting waveform and the limiting step is shown in Figure 5. If the limiting factor is taken as the resolution of the DAC, 0.58nm, it takes approximately 200 components (100 odd components) to reach the resolution limit as shown in Figure 6.

The iterative algorithm does waveform correction in the frequency domain. Initially, the coefficients of the Fourier components being used are set to their target amplitude and the response is found. The coefficients are then updated according to

$$D'_k = D_{n,k} + g\left(T_k - R_{n,k}\right)\left(\frac{D_{n,k} - D_{n-1,k}}{R_{n,k} - R_{n-1,k}}\right) \tag{5}$$

where D'_k will be the new input coefficients, D_{nk} are the current input coefficients, $D_{n-1,k}$ are the previous iteration's coefficients, R_{nk} are the current coefficients output from the modulator system, T_k are the target coefficients of the ideal synthesized waveform, and g is a gain coefficient taken as 0.2.[2] The n subscripts correspond to iteration number and the k subscripts are the coefficient number. Using a randomly generated sequence to simulate the system response of the modulators, 25 iterations were needed for convergence of the 200 component wave. Figure 6 shows the initial and final responses from this simulation.

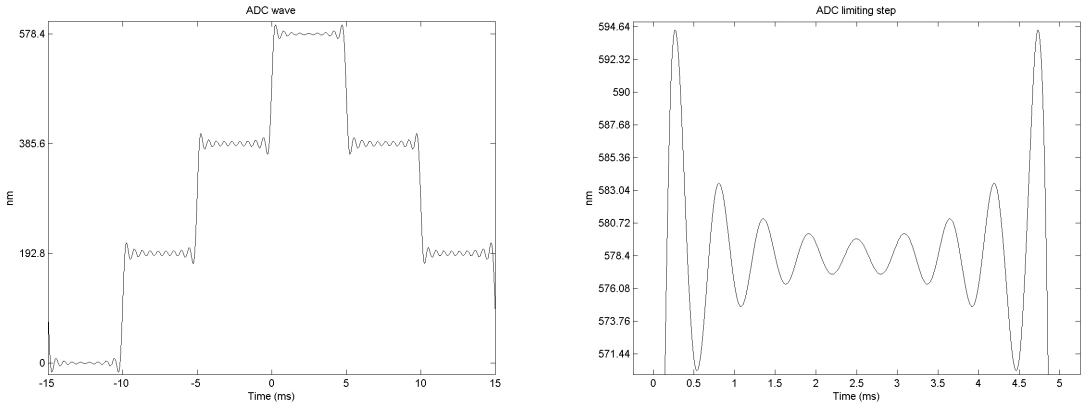

Figure 5. Waveform generated using 55 Fourier components. The portion of the wave that reached the resolution of the ADC is a shown on the right.

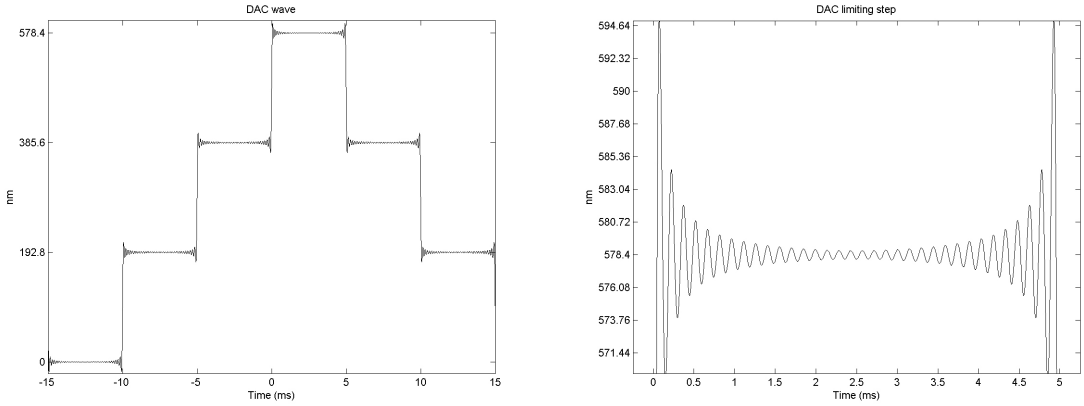

Figure 6. Same as Figure 5 but using the resolution of the DAC as the limiting factor (200 components). Note the improvement in reconstructig the ideal waveform compared to Figure 5.

6. FUTURE WORK

An optimized waveform has yet to be verified in hardware. Work towards accomplishing this goal will include reducing noise on the strain gauge readout and better determining an operation mode for the ADC. Operating the ADC under Linux would be optimal. If the current card cannot be run under Linux, a different ADC will be considered. A rough response curve has been obtained but more work is needed.

Once an optimized wave is found, a means to check and correct for drift at a specified time interval, synchronous or asynchronous, is desired. In this case, being able to read back the system response under Linux is mandatory. Because the algorithm corrects the driving components to produce the ideal output, reoptimization can occur at any time given the required hardware is in place.

7. CONCLUSION

The MROI fringe tracking beam combiner will use an optimized waveform to drive the modulators that aide in obtaining the required measurements for group delay tracking and correction of atmospheric aberrations. Through optimizing the waveform, the authors intend to produce a system stable for a period of time on the order of an observing night. This is done by correcting the driving waveform to account for the response of the system. Optimization will be done in the frequency domain. Much of the experimental setup has been complete

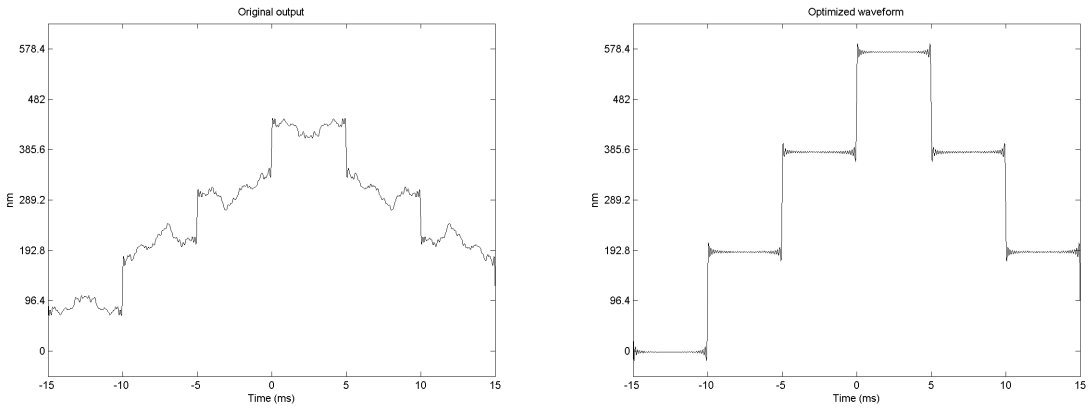

Figure 7. Optimization of a 200 component waveform using a randomly generated frequency response. The left figure shows the original response and on the right, the output after 25 iterations. The resulting waveform matches extremely well with Figure 6.

and is based around an embedded control system used to interface and drive the modulators. The number of components that will synthesize the waveform depends on the resolution of the hardware being used.

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